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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,117	05/30/2006	Jozef Pieter Van Gassel	NL 031406	5189

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EXAMINER	
SNYDER, STEVEN G	
ART UNIT	**PAPER NUMBER**
2184	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,117	VAN GASSEL ET AL.	
	Examiner	Art Unit	
	Steven G. Snyder	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is in response to application filed on May 30, 2006 in which claims 1 to 13 are presented for examination.

Status of Claims

Claims 1 to 13 are pending, of which claims 1, 9, and 13 are in independent form.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claim 5** recites the limitation "the optimum buffer memory value" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 1 describes an "optimum buffer size."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1 – 4, 6, and 9 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kever et al., U.S. Patent Application 2003/0145239 (hereinafter referred to as Kever) in view of Korst et al., U.S. Patent 6,061,732 (hereinafter referred to as Korst).**

Referring to claim 1, Kever discloses a method for adaptively minimising the total power consumption of an apparatus (paragraph [0008] describes how sections of cache memory may be turned on or off depending on the current needs of the system). Kever also discloses said method comprising the steps of determining an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate to/from said buffer memory, and adjusting the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal (paragraphs [0009] and [0010] describe how a monitor controls which section of memory is turned on or off based on signals from a software application indicating how much memory the application needs).

It is noted, however, that Kever does not specifically teach the memory sections being connected to a hard disk drive. Korst, however, achieves the aspect of a hard disk drive connected to a plurality of memory buffers (See storage medium 110 of Fig. 1 of Korst).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method and system of Kever's invention, as explained above, to include Korst's invention, wherein the memory sections would be connected to a hard disk drive. This would provide a means for permanently saving data temporarily stored in the buffer memories.

As per claim 2, the majority of the limitations of this claim have been noted in the rejection of claim 1 (See detail of claim 1 rejection above). Also, Kever discloses

the step of adjusting the buffer size comprises switching on memory banks and/or memory ICs of said buffer memory for increasing the size of said buffer memory, and switching off memory banks and/or memory ICs for decreasing said buffer memory (Fig. 1 and Fig. 2 show how switches S11 – S13 and S21 – S23 are used to control whether or not each memory array is powered (on) or not powered (off)).

Also, since this claim depends on claim 1, the motivation to combine Kever and Korst's inventions applies to this claim as well.

As per claim 3, the majority of the limitations of this claim have been noted in the rejection of claim 1 (See detail of claim 1 rejection above). Also, Kever discloses, in paragraph [0010], how an application may indicate how much memory the application needs.

It is noted, however, that Kever does not specifically teach determining a harddisk drive data rate, determining the stream bit-rate to/from the buffer memory, and determining the optimum buffer size having the lowest power consumption at the determined stream bit-rate. Korst, however, achieves the aspect of a scheduler being used for load balancing between a rate of reading from the hard disk and a stream bit rate associated with the buffer memory (See Korst column 2 lines 21 – 45 and column 5 line 66 – column 6 line 7).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method and system of Kever's invention, as explained above, to include Korst's invention, wherein a scheduler would determine data rates of the hard

disk and the buffer memory in order to determine the needed buffer size. This would provide a means for saving power by reacting to current conditions and only powering needed memory sections.

As per claim 4, the majority of the limitations of this claim have been noted in the rejection of claim 3 (See detail of claim 3 rejection above). Also, it is noted that Kever does not specifically teach how the optimum buffer size determination step comprises calculating optimum buffer size from a formula, looking up optimum buffer size in a look-up table, or measuring the minimum power consumption of the subsystem in a feedback loop controlling buffer size. Korst, however, achieves the aspect of an equation using the data rate of the hard disk along with the data stream bit rate to determine how much memory is necessary (See Korst column 4 line 56 – column 5 line 18).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method and system of Kever's invention, as explained above, to include Korst's invention, wherein the signals sent from the application to convey how much memory is needed would be based on the result of a formula. This would provide a simple means for determining how much memory is needed.

As per claim 6, the majority of the limitations of this claim have been noted in the rejection of claim 1 (See detail of claim 1 rejection above). Also, Kever discloses powering up extra memory banks and/or memory ICs when a new stream is admitted

(paragraph [0008] describes how power can be saved by turning off memory sections that aren't needed and turning on memory sections when other applications require it. Also, paragraph [0010] describes how applications may send signals to turn on or off memory sections while the application is running).

Also, since this claim depends on claim 1, the motivation to combine Kever and Korst's inventions applies to this claim as well.

Referring to claim 9, the limitations of this claim are equivalent to the limitations of the method of claim 1, except for the limitation of retrieving the data from the mass storage device (Korst's Fig. 1 shows a method for reading data stored in a hard disk). Also, since the remaining limitations are equivalent to claim 1, the rejection to claim 1 applies to this claim as well.

Also, since this claim depends on claim 1, the motivation to combine Kever and Korst's inventions applies to this claim as well.

As per claim 10, the majority of the limitations of this claim have been noted in the rejection of claim 9 (See detail of claim 9 rejection above). Also, Korst discloses, in Fig. 1, a system including a hard disk drive and buffer memory. As stated in the rejection to claim 1, the combination of Kever and Korst's inventions would create a system including a hard disk drive, buffer memory, and a circuit that controls the switching on and off of power to memory sections.

Also, the motivation to combine Kever and Korst's inventions, as stated in the rejection to claim 1, applies to this claim as well.

As per claim 11, the majority of the limitations of this claim have been noted in the rejection of claim 10 (See detail of claim 10 rejection above). Also, Korst discloses how buffer memory comprises SDRAM circuits having banks of memory adapted to be independently switched on/off (column 9 lines 65 – 66 describes how the buffers are usually implemented using RAM).

Also, since this claim depends on claim 10, the motivation to combine Kever and Korst's inventions, as stated in the rejection to claim 1, applies to this claim as well.

As per claim 12, the majority of the limitations of this claim have been noted in the rejection of claim 10 (See detail of claim 10 rejection above). Also, Korst discloses a scheduler function executable by the processing unit controls accessing the storage device and the buffer memory (Fig. 1 shows a scheduler 170 that is incorporated in the system and controls the transfer of data between the hard disk and the buffer memory).

Also, since this claim depends on claim 10, the motivation to combine Kever and Korst's inventions, as stated in the rejection to claim 1, applies to this claim as well.

Referring to claim 13, Kever discloses a computer-readable medium having embodied thereon a computer program for processing by a computer, the computer program comprising code segments for adaptively minimising the total power

consumption of a subsystem, and a code segment adjusts the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal (paragraph [0010] describes how an application sends signals to instruct the switching on or off of memory sections. Also, Kever discloses, in paragraph [0005], a microprocessor being used to monitor the system and switch memory sections on or off. It is known in the art that microprocessors carry out actions based on code segments).

It is noted, however, that Kever does not disclose a system comprising a mass storage device and a buffer memory. Kever also does not disclose a code segment for determining an optimum buffer size. Korst, however, discloses, in Fig. 1, a system including a mass storage device. Korst also achieves the aspect of determining an optimum buffer size based on a formula (See Korst column 4 line 56 – column 5 line 18).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method and system of Kever's invention, as explained above, to include Korst's invention, wherein the buffer memory is connected to a hard drive and the application uses an equation to determine an optimum buffer size. This would provide a means for the application to arrive at a conclusion about which memory sections should be switched on or off.

4. **Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kever in view of Korst, as applied to claims 1 – 4, 6, and 9 – 13 above, and further in view of Kling et al., U.S. Patent Application 2001/0003207 (hereinafter referred to as Kling).**

As per claim 5, the majority of the limitations of this claim have been noted in the rejection of claim 1 (See detail of claim 1 rejection above). Also, Kever discloses, in Fig. 1, memory sections that can be turned on or off. Further, Korst discloses, in column 2 lines 21 – 45 and column 5 line 66 – column 6 line 7, a scheduler being used for load balancing between a rate of reading from the hard disk and a stream bit rate associated with the buffer memory.

It is noted, however, that neither Kever nor Korst specifically teach using a ratio of the stream bit rate and the disk bit rate giving the duty cycle of the hard disk for calculating power consumption. Kling, however, achieves the aspect of monitoring power consumption by measuring the duty cycle (See Kling paragraph [0018]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method and system of the combination of Kever and Korst's inventions, as explained above, to include Kling's invention, wherein the duty cycle is measured in order to calculate the power consumption. This would provide a means for calculating power consumption in order to determine if one or more memory sections should be switched on or off.

5. **Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kever in view of Korst, as applied to claims 1 – 4, 6, and 9 – 13 above, and further in view of Yoshida, U.S. Patent 5,928,365 (hereinafter referred to as Yoshida).**

As per claim 7, the majority of the limitations of this claim have been noted in the rejection of claim 1 (See detail of claim 1 rejection above). It is noted that neither Kever nor Korst specifically teaches moving data stored in a memory section that is to be powered down into a memory that will remain powered. Yoshida, however, achieves the aspect of saving the contents of a memory section that will be switched off into another memory (See Yoshida column 9 line 53 – column 10 line 10).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method and system of the combination of Kever and Korst's inventions, as explained above, to include Yoshida's invention, wherein data in a memory section that is to be turned off is first saved in another memory area. This would provide a means for not losing the data currently in a memory section that is to be switched off.

6. **Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kever in view of Korst, as applied to claims 1 – 4, 6, and 9 – 13 above, and further in view of Falcon, Jr. et al., U.S. Patent 5,712,976 (hereinafter referred to as Falcon, Jr.).**

As per claim 8, the majority of the limitations of this claim have been noted in the rejection of claim 1 (See detail of claim 1 rejection above). It is noted, however, that neither Kever nor Korst specifically teaches adding the bit rates of all simultaneous streams to determine an optimum buffer size. Falcon, Jr., however, achieves the aspect of ensuring that the size of memory can support the maximum number of simultaneous streams (See Falcon, Jr., column 31 line 48 – column 32 line 7).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method and system of the combination of Kever and Korst's inventions, as explained above, to include Falcon, Jr.'s invention, wherein the bit rates of simultaneous bit streams would be added together when determining an optimum buffer size. This would provide a means for ensuring that the memory is large enough to handle the largest possible amount of data.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 7,100,013 discloses shutting off a section of memory.

U.S. Patent Application 2003/0154246 discloses a stream server incorporating a hard disk, buffer memory, and a scheduler.

U.S. Patent 5,898,880 discloses a power saving apparatus for a hard disk drive.

Japanese Patent Application 10340519 A discloses turning off the buffer memory associated with a hard disk.

Japanese Patent Application 60224186 A discloses cutting off power from memory cells.

Japanese Patent Application 5012895 A discloses memory cells that can be turned on or off.

Japanese Patent Application 2005025364 A discloses turning off power to each of a plurality of DRAM modules.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven G. Snyder whose telephone number is (571) 270-1971. The examiner can normally be reached on Mon. - Thurs. 9:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

S.S.

12/10/07

HENRY TSAI
SUPERVISORY PATENT EXAMINER